CLAIMS

1. A semiconductor device having a self-aligned contact, the semiconductor device comprising:

a plurality of conductive patterns formed to be adjacent to one another by sequentially stacking and patterning a first conductive layer and a mask layer on a particular underlying layer;

a first insulation layer filling a gap between adjacent conductive layer patterns such that the upper portion of each conductive layer pattern is exposed;

a second insulation layer having a spacer shape, the second insulation layer formed on the sides of each conductive layer pattern exposed above the first insulation layer; and

a second conductive layer filling a contact hole which is self-aligned with respect to the second insulation layers between adjacent conductive layer patterns and which passes through the first insulation layer.

2. The semiconductor device of claim 1, wherein the top of the first insulation layer is lower than the top of the first conductive layer of each conductive layer pattern.

3. The semiconductor device of claim 1, wherein the top of the first insulation layer is higher than the top of the first conductive layer of each conductive layer pattern.

4. The semiconductor device of claim 1, wherein an etching rate of the first insulation layer is larger than that of the second insulation layer.

5. The semiconductor device of claim 1, wherein the dielectric constant of the first insulation layer is smaller than that of the second insulation layer.

6. The semiconductor device of claim 1, wherein the first insulation layer is formed of a silicon oxide layer.

7. The semiconductor device of claim 1, wherein the second insulation layer is formed of a silicon nitride layer.

8. The semiconductor device of claim 1, further comprising a third insulation layer provided between the first insulation layer and the sides of each conductive layer pattern and between the second insulation layer and the side of the conductive layer pattern.

9. The semiconductor device of claim 8, wherein the third insulation layer is formed of a silicon nitride layer to a thickness of 50-200 Å.

10. The semiconductor device of claim 1, further comprising a fourth insulation layer provided on the surface of the underlying layer except for a portion contacting the second conductive layer and on the surfaces of the conductive layer patterns.

11. The semiconductor device of claim 10, wherein the fourth insulation layer is formed of a silicon nitride layer to a thickness of 50-200 Å.

12. The semiconductor device of claim 11, further comprising a field oxide layer formed on a certain portion of the surface of the underlying layer, wherein the second conductive layer is formed to at least partially contact the field oxide layer.

13. The semiconductor device of claim 11, further comprising a conductive pad layer formed on a certain portion of the surface of the underlying layer, wherein the second conductive layer is formed to contact the surface of the conductive pad layer.

14. The semiconductor device of claim 1, wherein the first conductive layer of each conductive layer pattern is a bit line, and the second conductive layer serves to

connect a storage electrode of a semiconductor capacitor to a semiconductor substrate.

15. The semiconductor device of claim 1, wherein the first conductive layer of each conductive layer pattern is a gate electrode, and the contact contacts the surface of a semiconductor substrate.

16. A method for fabricating a semiconductor device having a self-aligned contact, the method comprising:

forming a plurality of conductive layer patterns adjacent to one another by sequentially stacking a first conductive layer and a mask layer on a particular underlying layer and patterning the first conductive layer and the mask layer;

filling a gap between adjacent conductive layer patterns by depositing a first insulation layer on the surface of the underlying layer on which the conductive layer patterns are formed;

etching the entire surface of the first insulation layer to expose the upper portion of each conductive layer pattern;

forming a spacer of a second insulation layer on the sides of each exposed conductive layer pattern;

forming a contact hole self-aligned with respect to spacers so that the surface of the underlying layer between adjacent conductive layer patterns is exposed; and

forming a second conductive layer by filling the contact hole with a conductive material.

17. The method of claim 16, further comprising planarizing the surface of the first insulation layer after filling the gap between the adjacent conductive layer patterns with the first insulation layer.

18. The method of claim 16, further comprising forming an interlayer insulation layer, the surface of which is planarized, on the entire surface of the resultant structure obtained after forming the spacer of the second insulation layer.

19. The method of claim 16, further comprising forming an insulation layer used as an etching stopper on the entire surface of the resultant structure obtained after forming the conductive layer patterns.

20. The method of claim 19, further comprising forming a spacer of the insulation layer used as the etching stopper on the sides of each conductive layer pattern by etching the insulation layer used as the etching stopper.